

# VSIB Data I/O PCI Board

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## 1 Introduction

VSIB data I/O PCI board makes it possible to use conventional Linux PCs in continuously streaming high-throughput data acquisition and playback applications at data rates of 512 Mbits/s/PC and beyond. Furthermore, it is well-suited to data acquisition systems consisting of multiple PCs running in parallel and/or chained, resulting in both aggregate data rates of multi-Gbps and total on-line data volumes of several terabytes.

Because of board simplicity and low cost, and because of the use of standard PC hardware and low-cost IDE hard disks, even high-volume, high-throughput data acquisition systems can be realized at exceptionally low cost.

## 2 Features

VSIB has been designed as a standard half-size 32-bit, 33 MHz PCI expansion board. It is compatible with both 5V and 3.3V bus signalling with its “universal” dual-slot PCI card edge connector and

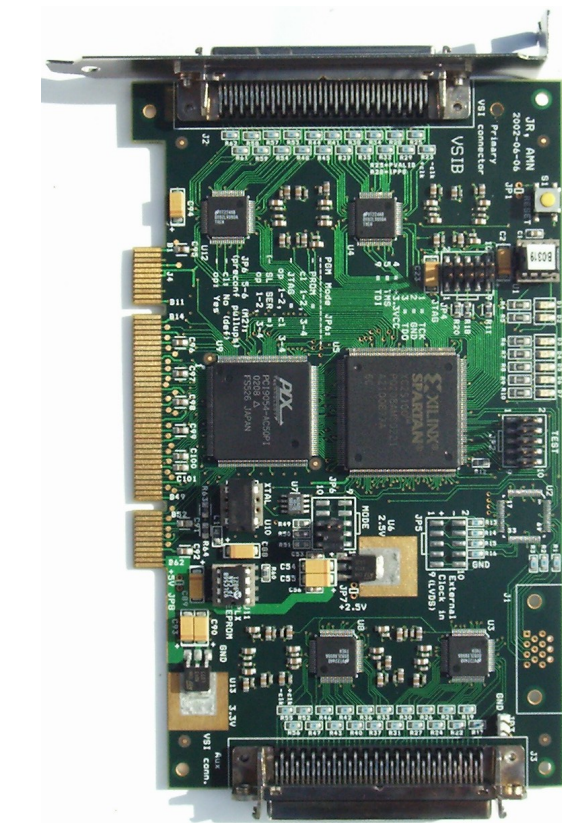


Figure 1: The VSIB data I/O PCI expansion board.

it can thus be used also in most 64-bit, 64 MHz PCI slots.

## 2.1 VSI Data I/O Connectors

The board features two bidirectional 32-bit parallel differential LVDS connectors which comply to the VSI, “VLBI Standard Interface” specification.<sup>1</sup> The connectors are female 80-pin MDR (“Miniature D Ribbon”) PCB connectors, as specified in the VSI-H standard. The main connector is located in standard PCI back plate, and the auxiliary (or chaining) connector is at the opposite end of the board.

In input mode, 32 parallel data bits are received and clocked in from the main VSI connector at the pace of an external clock. The maximum tested VSI clock frequency is 50 MHz. A copy of the data is reclocked and regenerated at the auxiliary VSI connector, facilitating arbitrary chaining of multiple VSIB boards.

In addition to data and clock, the board relies on an external synchronization signal (called “1pps”, one pulse per second in the VSI specification) to start data capturing operation. This allows multiple VSIB boards to start at precisely the same time. “1pps” signal is passed along in the main–aux signal chain delayed by the same amount as data, retaining synchronization information for boards participating in a VSI chain.

In output mode, the board sends and clocks out data at the auxiliary VSI connector at the clock rate received in main VSI connector clock pins. Again, data reproduction is started at the occurrence of an external synchronization signal.

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<sup>1</sup><http://web.haystack.edu/vsi/index.html>

## 2.2 On-Board Logic

Differential LVDS signals are processed with bus LVDS transceivers terminated with 100 $\Omega$  resistors at both ends, ensuring that cable connections are always correctly terminated. A Xilinx FPGA provides signal routing and processing, and a 4 kB buffer FIFO memory between VSI and PCI bus interface, ensuring continuous data flow regardless of PCI bus latencies.

The Xilinx logic allows selection of all 32 VSI data bits, or a subset of 16 or 8 (VLBI “Mark 5A” compatibility). It also allows skipping VSI input data words with a counter in the range of 1..65535. Both of these features can be used to direct a single VSIB to process a subset of the whole VSI data stream. For instance, four VSIB boards can be set up to repeatedly “demultiplex” four consecutive VSI data words to four VSIB boards in a chain, effectively reducing the data rate requirements for a single PC host to a quarter of the original data stream.

## 2.3 PCI Bus Interface

For connecting to any 32-bit, 33 MHz PCI expansion bus, VSIB utilizes a PLX bus-mastering interface chip. The chip enables high-throughput scatter/gather bus-master DMA transfers to and from PC main memory. Depending on motherboard chipset performance, VSIB has been demonstrated to sustain data transfers in excess of 700 MBits/s.

PC main memory, arranged in ring buffer

fashion, is used to allow VSIB to operate in conventional Linux operating environment without the need for any special real-time extensions. PCI bus interface hardware takes care of depositing data in large main memory ring buffer where Linux software can find it at its own pace.

### 3 Software Development

The VSIB board comes with a “vsib.o” Linux character-mode device driver and its source code. It utilizes Linux “bigphysarea=” memory management scheme for its large main memory ring buffer and presents a simple “open()/read()/write()/close()” paradigm for user software operation.

In addition to low-level drivers, a sample data collection application featuring TCP/IP remote control with “VSI-S” command messages is provided.

### 4 Typical Applications

While initially designed as a replacement for a 1inch magnetic tape instrumentation recorder (Honeywell/Metrum Model 69) used in radio astronomy VLBI measurements, the VSIB board can be used in a wide variety of instrumentation data acquisition tasks. A companion “VSIC” converter board is available to ease converting various digital interfacing standards such as TTL, RS422, RS485, differential ECL, and more to the standard differential LVDS 32-bit parallel format accepted by VSIB. The data rates supported

by VSIB are so high that recording for instance multiple uncompressed digitized video signals on a single PC is possible. For digital multi-channel audio on a single PC, VSIB offers the bandwidth capability of over 720 simultaneous audio channels digitized at 44 kHz and 16 bits.

### 5 Ordering Information

Model variants:

**VSIB-R** VSIB board with recording firmware.

**VSIB-P** VSIB board with playback firmware.

Board variants can be changed by just replacing the socketed firmware PROM.

### 6 Specifications

**Dimensions** 3.875x6.875in, standard half-size PCI expansion board.

**Connectors** 3M (or equivalent) 80-pin female MDR Miniature D Ribbon connectors, one main VSI connector (back plate), one auxiliary connector (opposite board side); differential LVDS signalling for 32 data bits, external clock, and external synchronization (start) signal. 10-pin ribbon cable connector with LVTTTL test signalling.

**Power Supply** +5VDC 1500mA max, 800mA typical. On-board regulators for +3.3VDC and +2.5VDC operating voltages.

**LVDS Interface** National Semiconductor DS92LV090 differential bus LVDS transceivers.

**Logic FPGA** Xilinx Spartan2 XC2S100-6PQ208C, with a socketed firmware PROM for easy firmware updates.

**PCI Interface** PLX PCI9054-50AC bus mastering PCI chip.

## Contact Information

VSIB boards are currently available for immediate delivery. For pricing please check our Web site at "<http://kurp-www.hut.fi/vlbi/instr/boards/>" or contact us directly:

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